Power-Efficient FIR Filter Architecture Design for Wireless Embedded System

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***Abstract*—This paper presents a novel approach for implementing power-efficient finite-impulse response (FIR) filters that requires less power consumption than traditional FIR filter implementation in wireless embedded systems. The proposed schemes can be adopted in the direct form FIR filter and achieve a large amount of reduction in the power consumption. By using a combination of proposed methods, balanced-modular techniques with retiming and separated processing data-flow scheme with modified canonical signed digit (CSD) representation, experimental results show that the proposed scheme reduce 76% power consumption of the original direct-form structure with slight area overhead.**

***Index Terms*—Canonical signed digit (CSD), direct form, embedded, finite-impulse response (FIR), power-efficient, retiming, wireless.**

I. Introduction

IN SEVERAL wireless hand-held systems, the finite-impulse response (FIR) filters are the indispensable parts among various image/video communication applications to reduce noise and to enhance the specific features. With a given specification, the dedicated filter is designed to fit in the applications and has the least effect of redundancy.

However, the previous designs of the dedicated filter architecture still have some drawbacks. The overhead of the subexpression sharing [1], [2] is a complicated routine like a chaotic adder tree. To keep timing correct, the substructure sharing will make the registers grow rapidly. Therefore, this approach is difficult for the hardware implementation. In addition, the advantage of the fixed coefficients can not be utilized by the folded architecture [3], [4]. Hence, the folded architecture loses the benefit in the chip area and the power consumption. The direct form and the transposed form [5], [6] usually represent the filter coefficients in the canonical signed digit from (CSD) to decrease the nonzero digits of the constant multipliers. At the same time, Firgen [5] and Laskowski [6] contributed to the elimination of the MSB sign-extension redundancy. However, the disadvantage is that the structural symmetry in the linear-phase frequency response can not be applied to transposed form filters designs.

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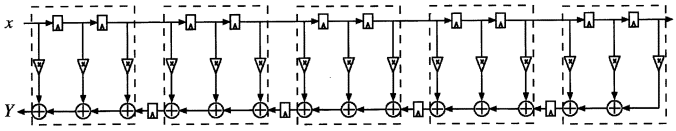

Fig. 1. Retimed direct form architecture.

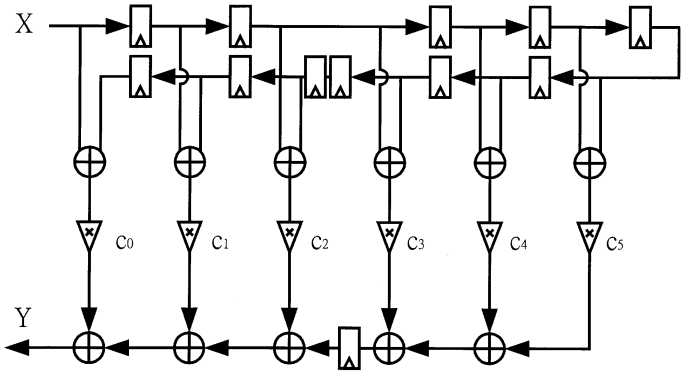

Fig. 2. Symmetrical Retimed linear-phase direct form architecture with 12 taps.

In this paper, we provide a solution to the problems described above by designing an FIR filter based on the architecture with modular design. The routing scheme is not very complicated and it still keeps the symmetric, and multiplier-less benefits. Besides, adding the proposed separated sign processing with modified CSD representation will have excellent results both in balancing critical-path delay and suppressing circuit transition.

II. Proposed Architecture

In this paper, the direct form of dedicated FIR with CSD coefficient representation is considered. There are four steps to reduce the power consumption.

A. Symmetrical Retimed Direct Form Architecture

Retiming method can decrease the critical path as the pipeline method but without increasing the latency of circuit. If the phase of the filter is linear, the symmetrical architecture

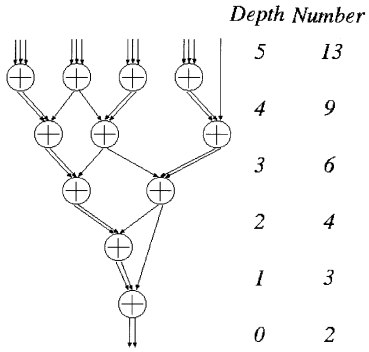

Fig. 3. Example of carry-save adder tree.

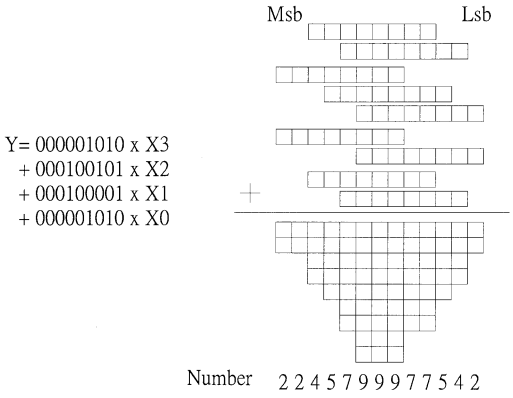

Fig. 4. Summation of partial products.

can be used to reduce the multiplier operation. Comparing Figs. 1 and 2, the number of multipliers can be reduced half after adopting the symmetrical architecture. The symmetrical retimed direct form architecture (RDFA) takes the advantage in speed and area, and it is the basic model to develop the proposed architecture.

B. Balanced Modular Architecture (BMA)

The same nonzero digits instead of the same numbers of coefficients are chosen, because the multiplier in each stage is not identical to each other. And a carry-save adder tree adopted with the same depth is used in the modular design. Since the Wallace tree uses the 3:2 compression ratio, the bit numbers of each bit plane are 9, 6, 4, 3, and 2 in the Wallace tree as shown in Fig. 3. An example to explain this situation is illustrated in Fig. 4, where the formula $Y = 000\,001\,010 \times X_3 + 000\,100\,101 \times X_2 + 000\,100\,001 \times X_1 + 000\,001\,010 \times X_0$ contains 9 nonzero coefficients digits. The maximal number of summation of partial products is 9, and the corresponding depth of the carry-save adder tree is 4. After considering these ideas, the resulted filter structure is displayed in Fig. 5.

C. Separated Signed Processing Architecture

The 2's complemented number representation for VLSI design will cause amounts of power consumption while the circuit transits frequently between positive and negative. For example, 0 in a 10-b 2's complemented number representation is 0 000 000 000 but -1 is 1 111 111 111. A lot of transitions will consume a large amount of power. Separated signed processing architecture (SSPA) separates the negative digits of coefficients from positive digits. Two accumulating paths for each sign are finally utilized, stored, and merged together. In order to avoid the transition between positive and negative caused by the input data, the filter input must be biased to a positive number instead of the sign-magnitude representation. These biases at the last stage of the accumulating path are deleted. As a result in Fig. 6, this design processes the biased input signal X in two different datapaths for each sign without any control. Eventually, the results positive part and negative part from the datapaths and the compensation bias are summed together to get the final result.

D. Modification to the CSD (MCSD) Representation

Separated signed processing will produce the unbalanced module. Although, the occurrences of positive and negative digits have the same probability, it is just the average statistics. The modification of the CSD representation is proposed to solve the problem. The concept is to modify the CSD representation to balance the positive and negative parts, and the number of nonzero digits is the same as before. For example, if the number of positive digits is much less than that of negative digits, then $10\bar{1}$ should be changed into 011 to increase the number of positive digits while decreasing the number of negative digits. Evidently the modified CSD coefficients result in a structure shown in Fig. 7 has higher utilization of hardware than the one in Fig. 6.

III. Comparisons and Discussions

This section shows an example for IS-95 WCDMA pulse shaping FIR filter. The ideal floating-point coefficients of an IS-95 WCDMA FIR filter with 33-taps for the third-generation cellular phone. From our power analysis the symmetrical retimed direct form architecture (SRDFA) just needs 47% power consumption compare with the original direct-form architecture. Applying BMA will reduce to 64% of original power. By combining SSPA with MCSD representation, the power consumption can be reduced to 78% of the original one. If the four schemes are adopted together, the power consumption can decrease to 24% original direct-form architecture. The simulation results are shown in Table I, Figs. 8 and 9.

Compared to the linear-phase direct form architecture for IS-95 WCDMA filters, the modularization obviously decreases the transition count as shown in Table II. When the FIR filter is fed with a sequence of randomly generated data, the result is similar. For the IS-95 WCDMA pulse shaping filter, adopting the proposed architecture can reduce the number of circuit transition to be 71.4%.

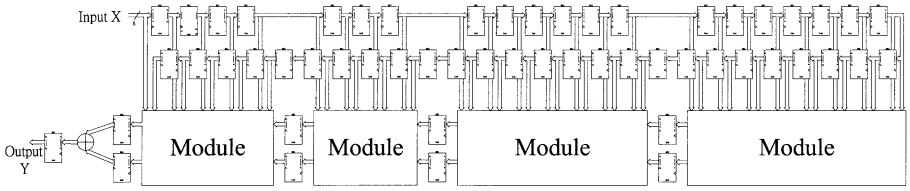

Fig. 5. Balanced modular FIR filter architecture.

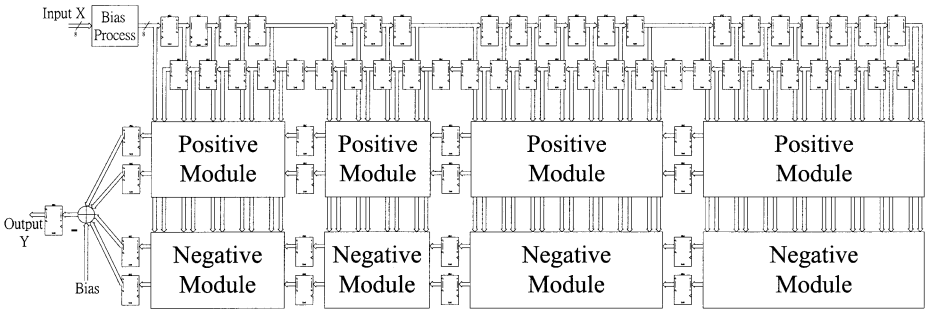

Fig. 6. Architecture with 4-level pipeline of pulse-shaping filter for IS-95 WCDMA.

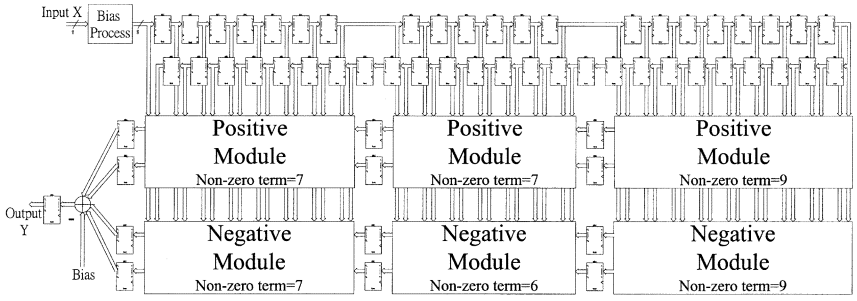

Fig. 7. The 3-level pipeline architecture of pulse-shaping filter for IS-95 WCDMA after adopting MCSD.

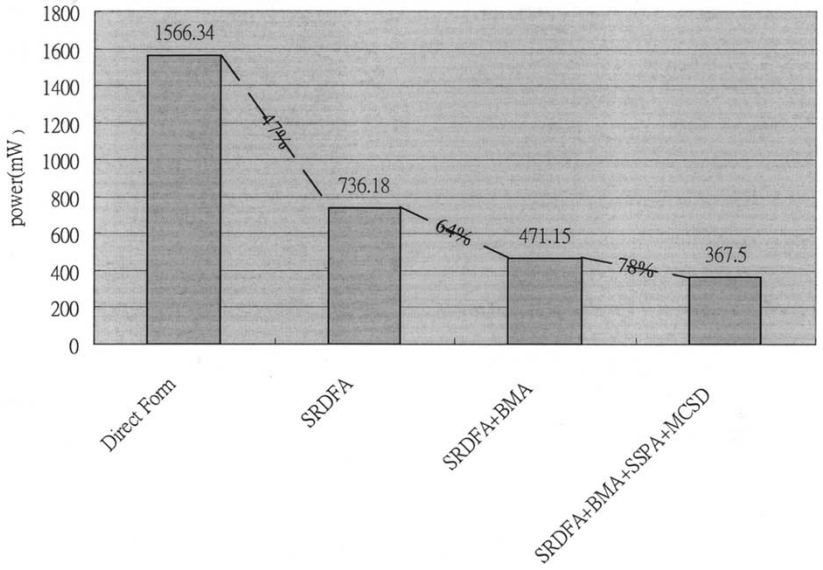

Fig. 8. Power comparison of the proposed four schemes.

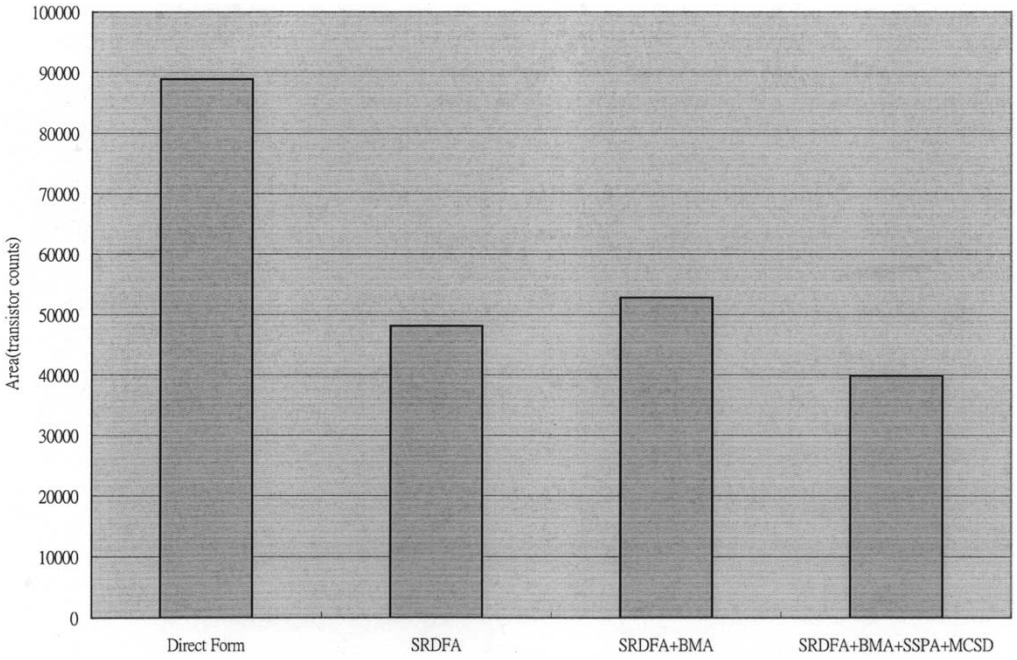

Fig. 9. Area comparison of the proposed four schemes.

TABLE I
COMPARISON RESULTS OF THE PROPOSED FOUR SCHEMES

	Direct Form	SRDFA	SRDFA+BMA	SRDFA+BMA+ SSPA+MCSD
power(mW)	1566.34	736.18	471.15	367.5
Area(transistor)	88923	48095	52805	39816
Vdd(v)	5	5	4	4
Frequency	50MHz	50MHz	50MHz	50MHz

TABLE II
THE NUMBER OF CIRCUIT TRANSITIONS OF THREE CASES

Case	Depth	Direct Form (Z)	SRDFA+ BMA (A)	SRDFA+BMA +SSPA+MCS D (B)	A/Z	B/A	B/Z
Simple channel data	5	9084792	7967036	7379256	0.877	0.926	0.812
Random input	5	23105843	20296336	18848949	0.878	0.929	0.816
IS-95 pulse-shaping filter	4	47719669	36933686	34074526	0.774	0.923	0.714
	5		40957155	38677669	0.858	0.944	0.810

IV. CONCLUSION

In this paper, a low-power architecture for dedicated linear phase FIR filter is proposed. Four schemes are suggested, including retimed structure, balanced modular architecture, separated signed processing data flow and modification of the CSD representation. From the experimental results, the proposed signal processing schemes reduce about ten to 30% circuits' transition in the accumulation path to achieve the maximum efficiency of hardware components. The proposed schemes not only address the linear-phase FIR filter, but also can improve the non linear-phase FIR filer.

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